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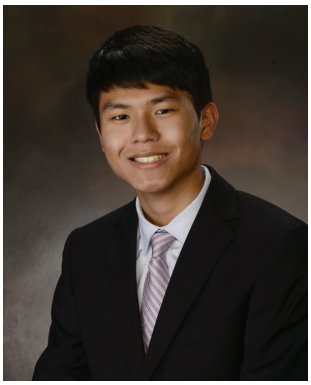
SUNGIL KIM



Sungil Kim was born in Daegu, South Korea on February 11, 1995. He and his family immigrated to the United States in 2009. He graduated from the Loveless Academic Magnet Program (LAMP) High School in Montgomery, Alabama. As the first generation to attend college, he entered Auburn University, majoring in Electrical and Computer Engineering. His extracurricular activities include membership in Phi Kappa Phi, Tau Beta Pi, Eta Kappa Nu, Pi Gamma Tau, IEEE, and ACM. His research interest is integrated circuit (IC) and systems design with an emphasis on low power or energy-efficient circuits and analog/RF IC design. Other interests include VLSI architectures for signal processing, bio-sensing, and biomedical electronics. As an undergraduate, he actively participated in research, teaching, and mentoring. As an independent researcher, he surveyed subthreshold circuit design and optimization for his honors thesis and has worked on his undergraduate research fellowship that focuses on analysis and forecast of stock market prices using signal and statistical analysis and genetic algorithm. Other collaborative research activities include being a research assistant in the VLSI Design/Automation laboratory at the University of Michigan, the Auburn University MRI center, Nanotech group, and Hill laboratory. He expects to graduate Summa Cum Laude with a Bachelor of Electrical Engineering (with Computer Option) on May 8, 2016. In the fall of 2016, he will seek a Ph.D. in Electrical Engineering with the focus on IC design.

ULTRA-LOW POWER AND VARIATIONS-TOLERANT SUBTHRESHOLD CIRCUIT DESIGN AND OPTIMIZATION

Modern electronics, whether medical imaging electronics, sensors, portable devices, or high-performance computers, are constrained by their power. It is well known that subthreshold circuit design where the supply voltage is less than the device threshold voltage can reduce the energy. That power reduction comes with significant performance drawback and susceptibility to process, voltage, and temperature (PVT) variations.

The energy saving and operation of the subthreshold circuit is demonstrated, and its advantages and limitations are discussed here. The analytical model to estimate circuit delay is also analyzed, particularly Alpha-Power Law. The estimated circuit delay by Alpha-Power Law is proven to be not effective in the subthreshold region because the subthreshold drain current exponentially depends on the gate-source voltage and subjects to PVT variations. To better estimate the circuit delay and understand the effect of variations in the subthreshold region, a variations-aware analytical model is proposed and verified through simulations. It is found that the circuit delay exponentially depends on $[\lambda(V_{DD2}\text{-}VD_{D1})/2mV_T]$, where λ is the drain-induced barrier lowering (DIBL) coefficient, m is the subthreshold slope factor, and V_T is the thermal voltage. In a 45nm BSIM bulk CMOS technology from the PTM model, λ is 0.001 and m is 27. With an average error of 15% in the subthreshold region, the proposed analytical model is proved to be a more effective measure of subthreshold circuit delay. Moreover, the effect of variations is analyzed, and the smaller technology nodes are found to have greater errors.

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To optimize both performance and power consumption, dual-threshold circuit design is explored, and a gate assignment algorithm is formulated using linear optimization (linear programming). The usage of both low threshold gates (fast and greater leakage power) and high threshold gates (slow and less leakage power) can improve performance while leakage power is reduced, and the circuit still operates properly.

Because wire capacitance does not scale with the supply voltage, and global wire delay is increasing with technology scaling, on-chip global interconnects causes significant performance degradation. Therefore, two techniques—repeater insertions and tapered interconnect driver—are discussed. In the subthreshold region where the driver delay dominates the overall interconnect delay, repeater insertions that superthreshold interconnects often use proved to be ineffective. An optimally sized, tapered driver can reduce up to 75% of the power-delay product. Also, the effect of interconnect length is discussed, and it is found that as interconnect length increases, a tapered driver is more effective.